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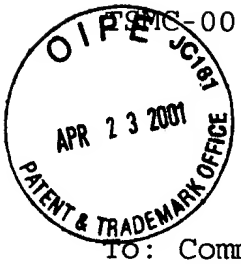

April 17, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/765,044 01/19/01

Chyi-Tsong Ni, Eric Su

METHOD TO PRODUCE POROUS OXIDE

Grp. Art Unit: 1762

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,054,206 to Mountsier, "Chemical Vapor Deposition of Low Density Silicon Dioxide films", describes a CVD process for producing low-density, porous oxides in a vacuum environment.

U.S. Patent 5,635,102 to Mehta, "Highly Selective Silicon Oxide Etching Method", describes a thermal oxide deposition process and etch methods.

U.S. Patent 5,824,375 to Gupta, "Decontamination of a Plasma Reactor Using a Plasma After a Chamber Clean", describes a chamber coating (seasoning) process before a CVD oxide deposition.

U.S. Patent 5,840,631 to Kubo et al., "Method of Manufacturing Semiconductor Device", describes a CVD silicon oxide formation method directly on a surface of a semiconductor substrate.

The following two U.S. Patents describe systems methods and apparatus for high temperature (at least about 500 to 800 degrees C) processing of semiconductor wafers:

1) U.S. Patent 6,114,216 to Yieh et al., "Methods for Shallow Trench Isolation".

2) U.S. Patent 6,099,647 to Yieh et al., "Methods and Apparatus for Forming Ultra-Shallow Doped Regions Using Doped Silicon Oxide Films".

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761